Fully Integrated Q-Band MMIC Transmitter and Receiver Chips using Resistive PHEMT Mixers

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Abstract

This paper describes the design of resistive PHEMT mixers and their application in fully integrated Q-band millimetre-wave monolithic receiver and transmitter chips, where LO power is limited. The design method has been verified with excellent measured performances over the RF frequency range of 36.5~40 GHz.

I. Introduction

Recently lots of MESFET and HEMT based mixers working in resistive mode have shown excellent performance with low inter-modulation and low conversion loss at microwave and millimetre wave frequencies [2-5]. Conventionally, the gate bias voltage of resistive mixer for optimum conversion loss is approximately the "turn on voltage", which is slightly below the "pinch-off voltage"; this is because this bias point allows the maximum channel resistance ratio when sufficient LO power is available [3,6,7]. However, in the design of single chip MMIC receivers or transmitters, on which the amplifier, mixer and oscillator are all integrated, the available LO power is restricted by chip size and cost constraints. When a mixer or converter is operating with low LO power, we find better conversion loss at an alternative bias point. In this paper we investigate this issue in detail. The investigation has been performed with resistive mixer analysis and verified by two different version of fully integrated receiver and an transmiter design and measurement.

II. Summary of resistive mixer analysis

The PHEMT device used for this work has 0.25 μm gate length with 2 fingers of 60 μm width. The transistor's maximum 52.5 mS of g_m is found at around +0.3V gate bias voltage. The drain to source resistance (R_{ds}), which is determined by the source and the drain ohmic contact resistance, the channel resistance controlled by the gate bias (V_{gs}) and the parasitic resistances, is a key parameter of the resistive mixer. Fig. 1 shows the modelled values of R_{ds} and C_{gs} (the gate to source capacitance) as functions of the gate voltage. First, an empirical equation for $R_{ds}(V_g)$ is fitted to the measurements of Fig. 1:-

$$R_{ds}\{V_{gs}(t)\} = \frac{1}{G_{ds}\{V_{gs}(t)\}} \approx 3800\left\{1.0038 - Tanh\left(1.514\left(V_{gs}(t) + 3.28\right) - 3.9\right) - 1\right\} \quad (1a)$$

$$C_{gs}\{V_{gs}(t)\} \approx \left\{0.014954\left(2.2 + Tanh\left[V_{gs}(t) + 0.525\right] - 0.0001537\right)\right\} \quad (1b)$$

$$V_{gs}(t) = V_{gs} + V_{LO}\cos(w_{LO}t + \theta) \quad (2)$$

Where V_{gs} is the gate DC bias voltage of resistive mixer, V_{LO} is the LO voltage at the gate terminal and ω_{LO} the local oscillator angular frequency. These two equations are forming the basis of the resistive mixer analysis presented here. The ratio of the maximum R_{ds} and the minimum R_{ds} (R_{max}/R_{min}) determines the conversion loss of the mixer (the higher the ratio is, the lower the conversion loss). The steeper R_{ds}-V_{gs} slope characteristics requires less LO-power. Unfortunately, the chosen PHEMT has shown very wide ΔV_{gs} range to swing very wide dynamic range of the R_{ds} within. The wide ΔV_{gs} range requires high LO power level to swing whole resistance dynamic range. From the empirical equations the maximum and minimum R_{ds} ratio vs the gate DC bias is drawn from repetitive calculation of R_{ds} as shown in Fig. 2. Fig.2

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can be easily converted to conversion loss given by [1] with the designed Y-type mixer.

$$C_L = 18.3\left(R_{\min}/R_{\max}\right)^{\frac{1}{3}} \qquad (3)$$

Note, however that these equations have ignored the gate source capacitance which is at its peak at minimum channel resistance.

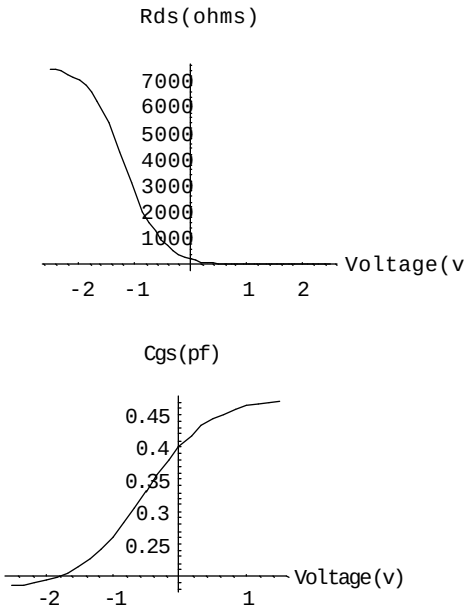

Fig. 1 The modelled values of R_{ds} and C_{ds} as functions of the gate voltage

It is apparent in Fig. 2 that the maximum resistance ratio or minimum conversion loss can be seen at near pinch-off bias point (point A) when LO power is high. At this point we can expect the minimum available mixer conversion loss of 2.6 dB using the equation (3) at Vgs = -1.2V and LO voltage 2.0 V (10 dBm at 50Ω load).

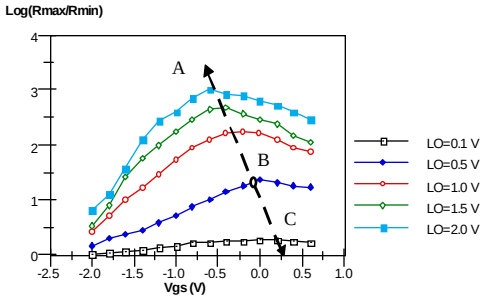

Fig. 2 Maximum and minimum source to drain resistance ratio according to applied DC gate bias voltage

But when LO power is low, the maximum resistance ratio point moves toward positive gate bias point (point C). At point B (at Vgs = -0.1V and -2dBm LO power at 50Ω load), the alternative minimum conversion loss of 8.3 dB is expected at the alternative maximum resistance ratio of 20. Now we will include the parasitic capacitance such as C_{gs} effect on conversion loss because the depletion area is spread horizontally, causing higher gate to source capacitance (C_{gs}) due to "zero" drain voltage. This increased gate-to- source capacitance usually allows the LO signal to couple to the drain, which is the RF input port and the IF output port. The LO signal coupling to the drain indicates not only poor isolations between ports, but also gives higher conversion loss due to LO leakage. This fundamental limit is given by [1]

$$C_{L(\min)} = 1 + 2\left(\frac{f_s}{f_c}\right)^2\left[1+\sqrt{1+\left(f_c/f_s\right)^2}\right] \qquad (4)$$

where f_c and f_s are cut-off frequency of the transistor (60GHz) and signal frequency (38GHz) respectively. With reference to the switching device model shown, the theoretically estimated fundamental limit to minimum conversion loss is 4.4 dB. This means that extra 1.8 dB conversion loss is added to the minimum available conversion loss of 2.6dB due to parasitic capacitance. The analysis shows that due to low LO power in fully integrated MMIC design, our practical design approach will give minimum conversion loss at the alternative optimum gate bias voltage around V_{gs} = -0.1V. Considering this fundamental limitation by C_{gs} and non-ideal R_{ds} (not zero to infinitive), conversion loss of 4.4 dB is achieved at -1.2V gate bias voltage when LO voltage is 2.0 V_{pp} or higher. But at low LO voltage of 0.5 V_{pp} , an extra 5.7 dB (8.3 dB - 2.6 dB) conversion loss is generated, so that total conversion loss at point B is calculated as 8.3dB + 1.8 dB = 10.1dB at V_{gs} =-0.1 V.

III. Verifications by fully integrated receivers and transmiter measurements

In this section our design approach and analysis are confirmed through the experimental results. While the receiver I and the transmiter are using a single-ended passive mixer topology with identical LO circuitry, the receiver II makes use of a PHEMT pair as

push-pull resistive element to implement harmonic receiver with identical passive mixer circuitry.

Receiver I : Fig.3 shows a microphotograph of the receiver type I (1.5x1.8mm). The conversion gain according to the resistive mixer gate bias voltage with fixed RF frequency (38 GHz) is shown in Fig.4a. It clearly shows that the channel resistance ratio is its alternative maximum at 0.1V, so that the alternative maximum conversion gain has been achieved at this bias point. This result agrees exactly to our expectation based on the channel resistance modelling. The result shows that the gain over the measured frequency range (32 GHz up to 40 GHz) is 8.5 ± 1.5 dB at the 0.1 V gate bias voltage with 4~5 GHz IF frequency.

Receiver II : This receiver uses a harmonic mixer technique using two mixers pumped in push-pull from an $F_{lo}/2$ signal. Fig.5 shows the microphotograph of the harmonic resistive mixer (the receiver II) which measures 1.6 x 1.9 mm^2.

An average conversion gain of the receiver II over IF frequency from 0.1 GHz to 14 GHz shown in Fig.6 is - 2.5 ± 1dB at 0.1 V V_{gs}. Fig. 6 shows the conversion loss of receiver II vs. the mixer gate bias voltage.

Up-converter : The microphotograph of the Q-band transmiter (1.7x2.0mm) is shown in Fig. 7. The mixer used here is similar to Receiver I, reconfigured for upconversion. Since the LO circuitry and RF amplifier are the same, the transmiter conversion loss can be directly compared with receiver I. The minimum conversion loss was observed in 0.0 V gate bias voltage as shown in Fig. 8, which again confirms that the mixer provides the minimum conversion loss well away from pinch-off. The transmiter exhibits an average conversion loss of 0dB over IF frequency range of 1~8 GHz at 0.0V mixer gate bias.

IV. Discussions and conclusions

This paper has described the design, analysis and performances of the two fully integrated receivers and a transmitter which are using resistive PHEMT mixers. The measured results confirm that the minimum conversion loss of the resistive mixer is not achieved at the conventional bias point due to low LO power. Experimentally and theoretically, the alternative optimum gate bias point has been investigated. With this design approach, high performance compact transmitter/receiver chips have been successfully demonstrated in the 36.5 to 40 GHz range.

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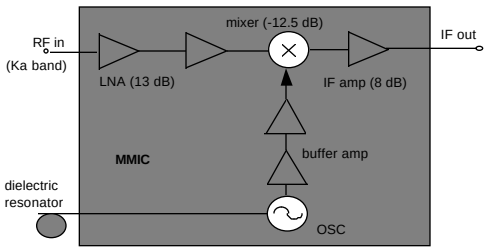


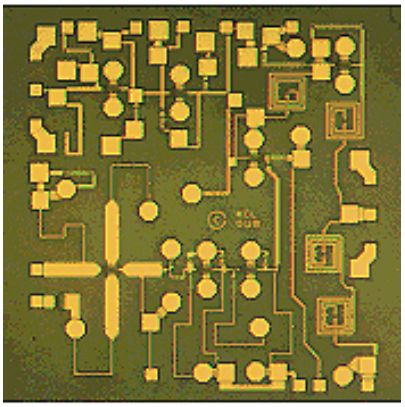
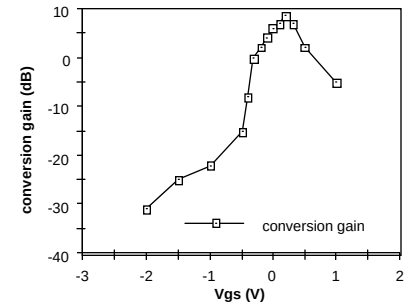


Fig.3 Fabricated receiver I microphotograph and block diagram



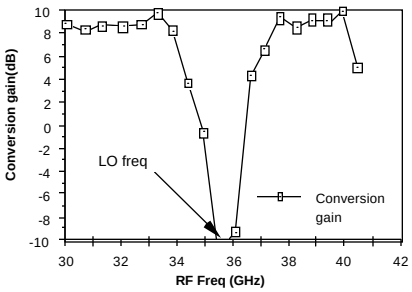


Fig.4 measured receiver conversion gain (a) conversion gain vs mixer gate bias (b) conversion gain vs RF freq

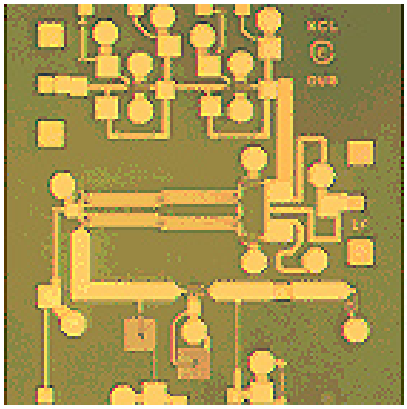
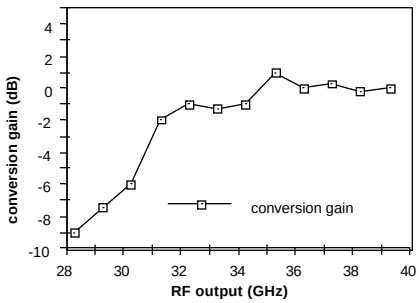


Fig.5 Microphotograph of the receiver II (using harmonically pumped resistive mixer)



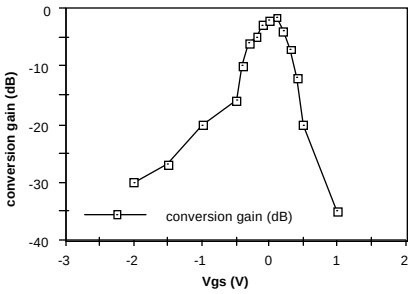


FIG. 6 Measured conversion gain of the receiver II (a) conversion gain over IF (b) conversion gain over V_{gs}

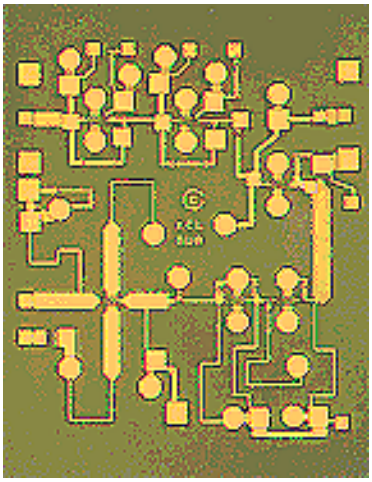
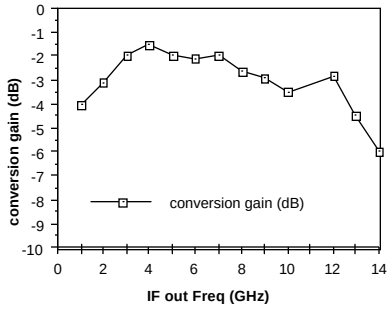


Fig. 7 Microphotograph for the Q-band transmiter



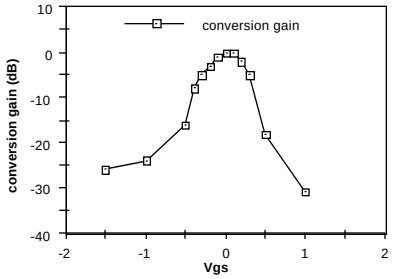


Fig. 8 Measured conversion loss of the transmiter (a) conversion gain vs IF (b) conversion gain vs V_{gs}